Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**ANODE**

**.070 x .070”**

**.087”**

**.087”**

**Top Material: Au**

**Backside Material: Au**

**Bond Pad Size: .070 X .070”**

**Backside Potential: CATHODE**

**Mask Ref: CMR3U-01**

**APPROVED BY: DK DIE SIZE .087” X .087” DATE: 11/10/21**

**MFG: CENTRAL SEMI THICKNESS .012” P/N: 1N5804**

**DG 10.1.2**

#### Rev B, 7/1